

Amended Claims

1. (withdrawn) A LVTSCR-like structure having one or more diodes formed in a p-well of the structure.

2. (currently amended) A method of increasing the holding voltage of an LVTSCR structure, comprising

~~that includes~~ forming an n-well and a p-well ~~formed~~ in a substrate,

~~a gate, forming~~ a first n+ region and a first p+ region ~~formed~~ in the n-well to define an anode ~~a high voltage node on one side of the gate, and~~

forming a second n+ region and a second p+ region ~~formed~~ in the p-well to define a cathode,

providing a gate between the anode and the cathode, and

~~low voltage node on the other side of the gate, the method comprising~~
forming an additional n+ region inside the p-well of the structure to define a p-n junction of a diode between the additional n+ region and the p-well, with the second p+ region forming a contact to the diode, and ~~and~~, the p-n junction being forward biased during normal operation by having said additional n+ region of the p-n junction located further from the high voltage node than the second p+ region, wherein the diode is located between the anode and the cathode.

3. (currently amended) A method of increasing the holding voltage of an LVTSCR structure comprising

forming ~~having~~ an anode in an n-well and a cathode in a p-well, the cathode being defined by an n+ region and a p+ region, comprising

forming at least one additional n+ region and at least one additional p+

region in the p-well to define at least one forward biased diode under normal operation in the p-well, the at least one forward biased diode being located between the anode and the cathode, thereby providing an alternative current path from anode to cathode through said at least one forward biased diode.

4. (currently amended) A method of claim 3, wherein the alternative current path defines a lower resistance current path than the current path defined by the p-well.
5. (canceled)
6. (canceled)
7. (canceled)
8. (canceled)
9. (currently amended) A method of claim 2, further comprising forming at least one additional p⁺ region and multiple additional n⁺ regions inside the p-well of the structure to define multiple diodes each with a p-n junction in the p-well, each diode being formed by ~~between~~ a p-type material and an n-type material, wherein the p-type material is defined by the p-well having one of the additional p⁺ regions or the second p⁺ region as diode contact, and wherein the n-type material is defined by one of the additional n⁺ regions.